Indian Institute of Information Technology Kalyani
(An Institute of National Importance under MoE, Govt. of India)
WEBEL IT Park Campus, West Bengal 741235, India

Course Structure and Syllabus

for

M. Tech.

in

VLSI and Embedded Systems

Dept. of Electronics and Communication Engineering
Indian Institute of Information Technology Kalyani
West Bengal 741235, India

Indian Institute of Information Technology Kalyani

(An Institute of National Importance under MoE, Govt. of India)
WEBEL IT Park Campus, West Bengal 741235, India

Course Structure

1st Year (Semester I)				
S. No.	*Subject Code*	*Title of the course*	*L-T-P*	*Credits*
1	MTVE101	Analog IC Design	3-0-0	3
2	MTVE102	Digital IC Design	3-0-0	3
3	MTVE103	Embedded Systems	3-0-0	3
4	MTVE104	Advanced Semiconductor Devices	3-0-0	3
5	MTVE111	Analog IC Design Laboratory	0-0-3	3
6	MTVE112	Digital IC Design Laboratory	0-0-3	3
7	MTVE15X	Elective-I	3-0-0	3
			Total credits	21

1st Year (Semester II)				
S. No.	*Subject Code*	*Title of the course*	*L-T-P*	*Credits*
1	MTVE201	Low Power VLSI	3-0-0	3
2	MTVE202	Mixed-Signal IC Design	3-0-0	3
3	MTVE203	VLSI Technology	3-0-0	3
4	MTVE211	Embedded System Laboratory	0-0-3	3
5	MTVE212	Mixed-Signal Laboratory	0-0-3	3
6	MTVE22X	Elective-II	3-0-0	3
7	MTVE23X	Elective-III	3-0-0	3
			Total credits	21

2nd Year (Semester III)				
S. No.	*Subject Code*	*Title of the course*	*L-T-P*	*Credits*
1	MTVE301	Project-I	-	20
			Total credits	20

2nd Year (Semester IV)				
S. No.	*Subject Code*	*Title of the course*	*L-T-P*	*Credits*
1	MTVE401	Project-II	-	20
			Total credits	20

Elective I:

1. Machine Learning
2. Optical Fibers, Components and Devices
3. Advanced Computer System Architecture
4. Principle of Nano-electronics and Devices
5. Antenna Engineering
6. Wireless communications
7. Mathematical methods
8. Architectural Design of ICs
9. VLSI Interconnects

---

10. VLSI for Telecommunication
11. Neural Networks and deep learning
12. MEMS & NEMS
13. Data Communications

Elective II, III:

1. RF CMOS circuits
2. CAD for VLSI
3. 5G and Wireless Technology
4. Nanoelectronics and Nanotechnology
5. VLSI Data Converter Design
6. Biosensors and Circuits
7. Digital Signal Processing and Applications
8. RF Design
9. Communication Infrastructure for IOT
10. Satellite Communication systems
11. Advanced Operating Systems
12. Technology CAD
13. Adaptive Systems and Signal Processing
14. Hardware-Software Codesign
15. VLSI for Cryptographic Design
16. Cyber-Physical Systems
17. System-on-Chip Design
18. VLSI Testing and Verification
19. Secure Communication
20. FPGA based System Design
21. Integrated Nano-photonics
22. Mobile communication and fading
23. Signal theory
24. Internet of Things
25. Information theory and coding
26. Quantum computing
27. Quantum AI
28. Operation research

Indian Institute of Information Technology Kalyani

(An Institute of National Importance under MoE, Govt. of India)
WEBEL IT Park Campus, West Bengal 741235, India

SEMESTER – I

Course Title : Analog IC Design
Course Code : MTVE101
Weekly contact : 3 – 0 – 0 (L – T – P)
Credit : 3

Module	Topics
M1	**Introduction:** Motivation for analog VLSI and mixed signal circuits in CMOS technologies and issues thereof.
M2	**CMOS Device Fundamentals:** Basic MOS models, device capacitances, parasitic resistances, substrate models, trans-conductance, output resistance, f_T, frequency dependence of device parameters.
M3	**Single Stage Amplifiers:** Common source amplifier, source degeneration, source follower, common gate amplifier, cascade stage.
M4	**Differential Amplifiers:** Basic differential pair, common mode response, differential pair with MOS loads, Gilbert Cell, device mismatch effects, input offset voltage.
M5	**Current Mirrors and Biasing Techniques:** Basic current mirrors, cascode current mirrors, active current mirrors, low current biasing, supply insensitive biasing, temperature insensitive biasing, impact of device mismatch.
M6	**Frequency Response of Amplifiers:** Miller effect, CS amplifier, source follower, CG amplifier, cascade stage, differential amplifier, Multistage amplifier.
M7	**Feedback:** Feedback topologies, effect of load, modeling input and output ports in feedback circuits
M8	**Noise:** Statistical characteristics, types of noise, single stage amplifiers, differential pair, noise bandwidth, impact of feedback on noise.
M9	**Operational Amplifiers:** Performance parameters, One-stage and two-stage Op-Amps, gain boosting, comparison, common mode feedback, input range, slew rate and high frequency Op-Amp, power supply rejection, noise in Op-Amps, buffered Op-Amps, differential output Op-Amps
M10	**Stability and Frequency Compensation:** Multi pole systems, phase margin, frequency compensation
M11	**Switched-Capacitor Circuits:** MOS sample and hold basics, CMOS sample and hold circuits, charge injection, switched-capacitor amplifier, switched-capacitor integrator

Reference Books:

1. "Analysis and Design of Analog Integrated Circuits", 4th Ed., Gray, Hurst, Wiley.
2. "Design of Analog CMOS Integrated Circuits", 2nd Ed., Razavi, B., McGraw Hill.
3. "CMOS Circuit Design, Layout and Simulation", 4th Ed., RJ Baker, IEEE.
4. "Analog Integrated Circuit Design", 2nd Ed., John D. A. and Martin K., Wiley.

Indian Institute of Information Technology Kalyani

(An Institute of National Importance under MoE, Govt. of India)
WEBEL IT Park Campus, West Bengal 741235, India

Course Title	**:**	**Digital IC Design**
Course Code	**:**	**MTVE102**
Weekly contact	**:**	**3 – 0 – 0 (L – T – P)**
Credit	**:**	**3**

Module	Topics
M1	**Introduction to VLSI:** Evolution of VLSI technology, Moore's Law, Types of ICs - Analog, Digital, Mixed-signal, Full-custom vs Semi-custom design, Design hierarchy and abstraction levels
M2	**VLSI Design Flow:** Front-end vs Back-end design, ASIC design flow steps: Specification, Architecture design, RTL design, Functional verification, Synthesis, Physical design, Tape-out
M3	**CMOS INVERTER:** Static CMOS Inverter: An Intuitive Perspective, Evaluating the Robustness of the CMOS Inverter: The Static Behavior, Noise Margins, Performance of CMOS Inverter: The Dynamic Behavior, Switching Threshold, Computing the Capacitance, Propagation Delay First-Order Analysis, Power, Energy, and Energy-Delay, Dynamic Power Consumption, Static Consumption, SPICE Diode Model, Static CMOS Design
M4	**Combinational Logic Circuits:** Complementary CMOS, Ratioed Logic, Pass-Transistor Logic, Dynamic CMOS Design, Dynamic Logic: Basic Principles, Speed and Power Dissipation of Dynamic Logic, Uses in Dynamic Design, Cascading Dynamic Gates, Logical Effort, Fan-In and Fan-Out Conditions
M5	**Design Perspectives:** How to Choose a Logic Style! Designing Logic for Reduced Supply Voltages, Representing Digital Data as a Continuous Entity, Representing Data as a Discrete Entity, Using Higher-Level Data Models
M6	**Sequential Logic Circuits:** Timing Metrics for Sequential Circuits, Classification of Memory Elements, Static Latches and Registers, the Bistability Principle, Multiplexer-Based Latches, Master-Slave Edge-Triggered Register, Low-Voltage Static Latches, Static SR Flip-Flops Writing Data by Pure Force, Dynamic Latches and Registers, Dynamic Transmission-Gate Edge-triggered Registers, C2MOS-A Clock-Skew Insensitive Approach, True Single-Phase Clocked Register (TSPCR), Alternative Register Styles, Pulse Registers, Sense-Amplifier Based Registers, Pipelining: An approach to optimize sequential circuits, Latch- vs. Register-Based Pipelines, NORA-CMOS-A Logic Style for Pipelined Structures, Non-Bistable Sequential Circuits, The Schmitt Trigger, Monostable Sequential Circuits, Astable Circuits, Choosing a Clocking Strategy

Reference Books:

1. "Digital Integrated Circuits: A Design Perspective", 4th Ed., Gray, Jan M Rabaey.
2. "Digital Integrated Circuit Design", Ken Martin, Oxford.

3. "Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication", Kaeslin, 2009.
4. "Digital Circuits And Design", S. Salivahanan, S. Arivazhagan.

Course Title : Embedded Systems
Course Code : MTVE103
Weekly contact : 3 – 0 – 0 (L – T – P)
Credit : 3

Module	Topics
M1	**Introduction:** Overview and Characteristics of Embedded Systems, Classification and Application Areas: CPU-only vs. CPU-accelerated embedded systems, Process of Embedded System Development, Components in an embedded system.
M2	**CPU-only Processor ARM CORTEX M3/M4:** What are the ARM Cortex -M processors?, Advantages of the Cortex -M processors, Applications of the ARM Cortex -M processors, Background and history. Introduction to Embedded Software Development, Technical Overview of ARM Cortex family, Processor type, Processor architecture, Instruction set , Block diagram, Memory system, Interrupt and exception support, Features of the Cortex -M3 and Cortex-M4 processors, Architecture… Introduction to the architecture, Programmer's model.
M3	**CPU-Accelerated Embedded Multiprocessors with Parallel and Pipelined Architectures:** Why multiprocessors?, Categories of multiprocessors, MPSoCs and shared memory multiprocessors, Heterogeneous shared memory multiprocessors , Accelerators, Accelerator performance analysis. Parallel And Pipelined Architectures, Characterizations Of Parallelism, Microscopic vs Macroscopic, Examples Of Microscopic Parallelism, Examples of Macroscopic Parallelism, Symmetric Vs. Asymmetric. A Modern Supercomputer and a GPU, ARM CORTEX M3 and NVIDIA A100 GPU comparison.
M4	**Operating System (OS) and Language:** Linux: Embedded System targets open-source Linux distributions, with Ubuntu 22.04 being the primary recommendation. Low-latency kernel: A key requirement for optimal performance is using a low-latency Linux kernel and disabling power-saving features. Containerization: Embedded System is designed to be deployed in containerized environments like Docker, RedHat: A RedHat Enterprise Linux (EL7/8) version is also supported through the k8s repository on GitHub for deployment using Kubernetes. Architecture: Intel X86 / ARM Cortex architectures, Languages: C and C++: These are the primary programming languages for the ES development, Python to be used for tooling, Continuous Integration (CI) and configuration.
M5	**PERIPHERAL INTERFACING:** General-purpose I/O, General-purpose Timers, Real-time Clock (RTC), Direct Memory Access (DMA), Analog-to-Digital Converter

	(ADC), Digital-to-Analog Converter (DAC), Serial Communication interface such as UART, I2C, SPI, Ethernet, CAN etc..
M6	**Design a cost-effective real-world embedded system with appropriate hardware/software components:** AI on 5G/6G USE CASE on miniaturised embedded 5G system ; Driving Innovation in 6G Wireless Technologies: The OpenAirInterface Approach; Qualcomm Dragonwing X100 ASIC Accelerator Card, 5G accelerated by the Xilinx FPGA T1 Telco card, Nvidia GPU Hosted AI-on-5G, Comparison between X100, T1 Telco and GPU Accelerated AI on 5G, Software Simulation : Open Air Interface (OAI), Hands-on tutorials, Core Network Hands-on Tutorial, RAN Hands-on Tutorial.

Reference Books:

1. "The Definitive Guide to ARM Cortex -M3 and Cortex -M4 Processors ", 3rd Ed., Joseph Yiu, Newnes, 2013.
2. "ARM System Developer's Guide : Designing and Optimizing System Software", A. N. Sloss, D. Symes, and C. Wright, Elsevier, 2004.
3. "Embedded Systems with Arm Cortex-M3 Microcontrollers in Assembly Language and C", Y. Zhu, E-Man Press LLC, 3rd edition, 2018.
4. "Essentials of Computer Architecture", 3rd Ed., Douglas Comer, CRC Press, 2024.

Course Title : Advanced Semiconductor Devices
Course Code : MTVE104
Weekly contact : 3 – 0 – 0 (L – T – P)
Credit : 3

Module	Topics
M1	**Semiconductor Electronics:** Semiconductor Materials, Band Model of Solids Thermal-Equilibrium Statistics, Carriers in Semiconductors, Drift Velocity, Mobility and Scattering, Drift & Diffusion Current, Device: Hall-Effect
M2	**Metal-Semiconductor Contacts and P-N Junctions:** Metal-Semiconductor junctions, Current-Voltage Characteristics, Surface Effects. The pn junction, Step Junction, Linearly Graded Junction, Heterojunctions, Reverse-Biased p-n junctions and break down mechanism. Generation and Recombination
M3	**Field-Effect Transistors (MOSFETs) and Its 1st order I-V Model:** MOS Capacitor, Flat Band Voltage, Oxide and Interface Charge, High and Low Frequency C-V Characteristics, Basic MOSFET behavior, Threshold Voltage Model, 1st Order I-V Model.

M4	**Short Channel Effects and 2nd Order I-V Model:** Moore's law, Technology nodes and ITRS, Physical & Technological Challenges to scaling short-channel effects: velocity saturation, device degradation, channel length modulation, body bias effect, threshold adjustment, mobility degradation, subthreshold current, hot carrier effects, velocity overshoot, high field effects in scaled MOSFETs, substrate current and effects in scaled MOSFETS
M5	**Nonconventional MOSFETs, Advanced Nano-electronics devices & nano-materials:** High-k/metal gate, high mobility MOSFETS, SOI, Multi-gate MOSFETs, Basics of FinFET and Gate-All-Around (GAA) transistor, 0D, 1D, 2D nanomaterials & bulk materials, their characterization techniques like FESEM, TEM, XRD, XPS, Raman & FTIR spectroscopy

Reference Books:

1. Physics of Semiconductor Devices by S. M. Sze and Kwok K. Ng, 3rd Edition, (John Wiley & Sons, 2002)
2. Semiconductor Physics and Devices by Donald A. Neamen, 3rd Edition, Mc Graw Hill, 2003
3. Microelectronic circuits by Adel S. Sedra & Kenneth C. Smith, Oxford university press, 2004
4. Fundamentals of Nanoelectronics by Hanson, Pearson
5. Robert F. Pierret, "Semiconductor Device Fundamentals", Pearson Education, 2006

Course Title : Machine Learning
Course Code : MTVE151
Weekly contact : 3 – 0 – 0 (L – T – P)
Credit : 3

Module	Topics
M1	**Introduction:** Machine learning (ML) definition, types of Machine Learning- supervised, unsupervised, semi-supervised, hypothesis function, hypothesis space, input and output as vectors, training data, test data, components of a machine learning system, various applications of ML
M2	**Evaluation Measures:** Accuracy, Precision, Recall, F-measure, Sensitivity, Specificity, Macro F1 score and weighted F1 score, Sampling, Bootstrapping and ROC, Hypotheses Testing K-fold cross validation, Likelihood Functions
M3	**Computational/ Machine Learning Theory:** Error Function, Problem of choosing order of M of the polynomial model selection, Theory of Generalization, Generalization

	and over-fitting, Bias-Variance, Trade-offs Overfitting, Regularization and Validation, Cross Validation, L1 Regularization or Lasso Regularization, L2 Regularization or Ridge Regularization, PAC Learnability and VC Dimensions
M4	**Instance-based Learning:** k-Nearest Neighbour (kNN) Classifier, Voronoi Diagram and Distance-Weighted kNN, Distance Metrics and Curse of Dimensionality, Computational Complexity: Condensing and High Dimensional Search (kd-tree)
M5	**Linear Model and Regression:** Linear Regression, Ridge Regression, Lasso [3L] Basic classification Models– Regression-based Classification, Logistic Regression, Regression with Regularization KNN [4L] Feature Extraction and Dimensionality Reduction: Purpose of feature extraction, Principal Component Analysis, Linear Discriminant Analysis
M6	**Clustering:** K-means, K-medoids, Hierarchical, Spectral [4L] Statistical Learning theory, Introduction to Reinforcement Learning. DBSCAN. - Dimensionality Reduction: PCA, t-SNE
M7	**Support Vector Machines:** Decision Boundary, hyperplane. Max Margin of Linear Classifiers, Support Vector: Optimization and Primal-Dual Problem, Lagrange Multiplier Method, Soft Margin and Non-linear SVM, Non-Linear to Linear Transformation, Dimensionality Reduction, Kernel Machines and Kernel Trick. Radial Basis Functions, E-M Algorithm and Gaussian Mixture Model.
M8	**Ensemble and Boosting Learning Method:** Bagging and Boosting, Adaboost, Gradient Boosting, Random Forest [4L] Unsupervised Learning
M9	**Artificial Neural Networks:** Biological motivation, Basic models of ANN, Nonlinear Model of a Neuron, Feed forward Neural Networks, Perceptron training rule, delta rule and Gradient Descent. Backpropagation (BP) algorithm for hidden layer, Extending BP to ANN with multiple hidden layers, Stochastic Gradient Descent, Hypotheses Space, Inductive Bias and Convergence. Variants of Neural Network Structures Shallow vs. Deep Neural Networks, Deep learning vs. traditional machine learning, Greedy layer-wise pretraining and fine tuning, Comparison of various activation functions such as Threshold, Sigmoid, Relu, Tanh
M10	**Recurrent Neural Networks:** Introduction to Recurrent Neural Networks, Training of RNN, Long Short Term Memory
M11	**Switched-Capacitor Circuits:** MOS sample and hold basics, CMOS sample and hold circuits, charge injection, switched-capacitor amplifier, switched-capacitor integrator

Reference Books:

1. Yaser S. Abu-Mostafa, Malik Magdon-Ismail, Hsuan-Tien Lin; Learning From Data, First Edition, AML Book, 2012.
2. Ethem Alpaydin; Introduction to Machine Learning, Third Edition, The MIT Press, September 2014.
3. Peter Flach, Machine Learning, Cambridge University Press, 2012
4. Kevin P. Murphy; Machine Learning: A Probabilistic Perspective, MIT Press, 2012.

Indian Institute of Information Technology Kalyani

(An Institute of National Importance under MoE, Govt. of India)
WEBEL IT Park Campus, West Bengal 741235, India

Course Title	**:**	**Analog IC Design Laboratory**
Course Code	**:**	**MTVE111**
Weekly contact	**:**	**0 – 0 – 3 (L – T – P)**
Credit	**:**	**3**

List of Experiments:

Exp. No.	Topics
1	IV Characteristics of PMOS and NMOS, λ calculation, and g_m/I_D vs. V_{GS} Plot
2	Design, Simulation and Layout of CMOS Inverter
3	Design, Simulation and Layout of Cascode Current Mirror
4	Design, Simulation and Layout of CS Amplifier and Source Follower
5	Design, Simulation and Layout of Cascode Amplifiers
6	Design, Simulation and Layout of Folded Cascode Amplifiers
7	Design, Simulation and Layout of Active Load CMOS Op-Amp
8	Design, Simulation and Layout of Two Stage CMOS Op-Amp
9	Design, Simulation and Layout of CMOS Op-Amp Compensation
10	Design, Simulation and Layout of Switched Capacitor Circuits
11	Mini Project on Analog IC Design

Reference Books:

1. "Analysis and Design of Analog Integrated Circuits", 4th Ed., Gray, Hurst, Wiley.
2. "Design of Analog CMOS Integrated Circuits", 2nd Ed., Razavi, B., McGraw Hill.
3. "CMOS Circuit Design, Layout and Simulation", 4th Ed., RJ Baker, IEEE.
4. "Analog Integrated Circuit Design", 2nd Ed., John D. A. and Martin K., Wiley.

Indian Institute of Information Technology Kalyani

(An Institute of National Importance under MoE, Govt. of India)
WEBEL IT Park Campus, West Bengal 741235, India

Course Title	**:**	**Digital IC Design Laboratory**
Course Code	**:**	**MTVE112**
Weekly contact	**:**	**0 – 0 – 3 (L – T – P)**
Credit	**:**	**3**

List of Experiments:

Exp. No.	Topics
1	Design, Simulation and Implementation of 4-bit Adder on FPGA Boolean Board
2	Design, Simulation and Implementation of 4-bit Up/Down Counter on FPGA Boolean Board
3	Design, Simulation and Implementation of Sawtooth Wave Generator on FPGA Boolean Board
4	Design, Simulation and Implementation of 4-bit modular addition on FPGA Boolean Board
5	Design, Simulation and Implementation of FSM-based Sawtooth Wave Generator on FPGA Boolean Board
6	Design, Simulation and Implementation of Triangular Wave Generator on FPGA Boolean Board
7	Design, Simulation and Implementation of Multiplexer on FPGA Boolean Board
8	Design, Simulation and Implementation of ALU on FPGA Boolean Board
9	Design, Simulation and Layout of Universal Logic Gates
10	Design, Simulation and Layout of Flip-Flops
11	Mini Project on Digital IC Design

Reference Books:

1. "Digital Integrated Circuits: A Design Perspective", 4th Ed., Gray, Jan M Rabaey.
2. "Digital Integrated Circuit Design", Ken Martin, Oxford.
3. "Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication", Kaeslin, 2009.
4. "Digital Design and Verification using Verilog & Systemverilog", Sanjay Churiwala, Usha Mehta, Vaishali Dhare, Wiley, 2025.

SEMESTER – II

Course Title : Low Power VLSI
Course Code : MTVE201
Weekly contact : 3 – 0 – 0 (L – T – P)
Credit : 3

Module	Topics
M1	**Introduction:** Need for Low power VLSI Circuits, Low Power Design Techniques at different Hierarchical levels, Overview MOS Inverter, Delay Estimation, Power-Delay Trade-off
M2	**Sources of Power Dissipation:** Dynamic Power Dissipation: Short Circuit Power, Switching Power, Glitching Power; Static Power Dissipation, Degrees of Freedom
M3	**Supply Voltage Scaling Approaches:** Device feature size scaling, Multi-Vdd Circuits, Architectural level approaches: Parallelism, Pipelining, Voltage scaling using high-level transformations, Dynamic voltage scaling, Power Management
M4	**Switched Capacitance Minimization Approaches:** Hardware Software Tradeoffs, Bus Encoding, Two's complements verses Sign Magnitude, Clock Gating, Architectural optimization, Clock Gating, Logic styles
M5	**Leakage Power Minimization Approaches:** Variable-threshold-voltage CMOS (VTCMOS) approach, Multi-threshold-voltage CMOS (MTCMOS) approach, Power gating, Transistor stacking, Dual-Vt assignment approach (DTCMOS)
M6	**Special Topics:** Adiabatic Switching Circuits, Battery-aware Synthesis, Variation tolerant design

Reference Books:

1. Sung Mo Kang, Yusuf Leblebici, CMOS Digital Integrated Circuits, Tata McGraw Hill
2. Neil H. E. Weste, K. Eshraghian, Principles of CMOS VLSI Design, 2nd Ed., Addison Wesley
3. A. Bellamour, M. I. Elmasri, Low Power VLSI CMOS Circuit Design, Kluwer Academic, 1995
4. Anantha P. Chandrakasan and Robert W. Brodersen, Low Power Digital CMOS Design, Kluwer Academic Publishers, 1995

Course Title : Mixed-Signal IC Design
Course Code : MTVE202
Weekly contact : 3 – 0 – 0 (L – T – P)
Credit : 3

Module	Topics
M1	**Introduction:** Signals, analog filter, digital filter, sampling, and aliasing
M2	**Op-Amp:** One-stage Op-Amp, two-stage Op-Amp, gain boosting, common-mode feedback, high-slew rate Op-Amp, Gilbert Cell
M3	**Frequency Compensation:** Multi-pole systems, phase margin, dominant-pole compensation, shunt-capacitance compensation, Miller compensation, pole-zero compensation, feed-forward compensation
M4	**Nonlinear Analog Circuits:** Characterization of comparators, basic CMOS comparator design, comparator DC performance, transient response, propagation delay, minimum input slew rate, clocked comparators
M5	**Switched-Capacitor Circuits:** Sampling switches, switched-capacitor circuits, design of switched capacitor amplifiers and integrators
M6	**ADC & DAC:** Basics of analog-to-digital converter (ADC) and digital-to-analog converter (DAC), Nyquist rate ADC including flash, interpolating, folding flash, SAR, and pipelined architectures; Nyquist rate DAC including voltage, current, and charge mode converters; oversampled ADC and DAC
M7	**Oscillators:** Ring oscillator, LC oscillator, voltage-controlled oscillator (VCO)
M8	**PLL:** Basic PLL topology, dynamics of simple PLL, phase detector, phase frequency detector, loop filter, charge pump PLL
M9	**Layout and Packaging**: General layout considerations, design rules, antenna effect, analog layout techniques, multifinger transistors, shallow trench isolation issues, well proximity effects, reference distribution, passive devices, interconnects, pads, ESD protection, substrate coupling, and packaging

Reference Books:

1. "CMOS Mixed-Signal Circuit Design", 2nd Ed., R. Jacob Baker, Wiley
2. "Design of Analog CMOS Integrated Circuits", 2nd Ed., Razavi, B., McGraw Hill
3. "CMOS Circuit Design, Layout, and Simulation", 4th Ed, RJ Baker, IEEE
4. "Introduction to CMOS Op-Amps and Comparators", 2nd Ed., R. Gregorian, Wiley

---

Course Title	**:**	**VLSI Technology**
Course Code	**:**	**MTVE203**
Weekly contact	**:**	**3 – 0 – 0 (L – T – P)**
Credit	**:**	**3**

Indian Institute of Information Technology Kalyani

(An Institute of National Importance under MoE, Govt. of India)
WEBEL IT Park Campus, West Bengal 741235, India

Module	Topics
M1	**Introduction:** History of IC's; Operation & Models for Devices of Interest: CMOS and MEMS, Front End of Line (FEOL), Back End of Line (BEOL)
M2	**Electronic Materials and Clean Room Environment:** What Crystal Structures, Defects in Crystals, Si, Poly Si, Si Crystal Growth, Definition of clean room, Need of Clean Room, RCA cleaning of Si
M3	**Oxidation:** Dry and Wet Oxidation, Kinetics of Oxidation, Oxidation Rate Constants, Dopant Redistribution, Oxide Charges, Device Isolation, LOCOS, STI, Oxidation System
M4	**Lithography:** Overview of Lithography, Radiation Sources, Masks, Photoresist, Components of Photoresist Optical Aligners, Resolution, Depth of Focus, Advanced Lithography: E-beam Lithography, X-ray Lithography, Ion Beam Lithography
M5	**Diffusion and Ion Implantation:** Pre-Deposition and Drive-in Diffusion Modelling, Dose, 2-Step Diffusions, Successive Diffusion, Lateral Diffusion, Series Resistance, Junction Depth, Irvin's Curves, Diffusion System. Problems in Thermal Diffusion, Advantages of Ion Implantation, Applications in ICs, Ion Implantation System, Mask, Energy Loss Mechanisms, Depth Profile, Range & Straggle, Lateral Straggle, Dose, Junction Depth, Ion Implantation Damage, Post Implantation Annealing, Ion Channeling, Multi Energy Implantation
M6	**Thin Film Deposition:** Physical Vapor Deposition: Thermal evaporation, Resistive Evaporation, Electron beam evaporation, Laser ablation, Sputtering. Chemical Vapor Deposition: Advantages and disadvantages of Chemical Vapor deposition (CVD) techniques over PVD techniques, reaction types, Boundaries and Flow, Different kinds of CVD techniques: APCVD, LPCVD, Metallorganic CVD (MOCVD), Plasma Enhanced CVD, etc.
M7	**Etching:** Anisotropy, Selectivity, Wet Etching, Plasma Etching, Reactive Ion Etching
M8	**Metallization/Interconnects:** Overview of Interconnects, Contacts, Metal gate/Poly Gate, Metallization, Problems in Aluminum Metal contacts, Al spike, Electromigration, Metal Silicides, Cu metal lines, Multilevel Metallization, Planarization, Inter Metal Dielectric
M9	**Process and Packaging:** NMOS, CMOS process, SOI process, 3D IC Process, Packaging

Reference Books:

1. S. M. Sze, "VLSI Technology", 2nd Edition, McGraw Hill, 2003.
2. J. Plummer, M. Deal and P. Griffin, "Silicon VLSI Technology", 1st Edition, Pearson Education, 2009.
3. S. M. Sze and May, "Fundamentals of Semiconductor Fabrication", 2nd Edition, Wiley, 2004.

Indian Institute of Information Technology Kalyani

(An Institute of National Importance under MoE, Govt. of India)
WEBEL IT Park Campus, West Bengal 741235, India

Course Title	**:**	**RF CMOS Circuits**
Course Code	**:**	**MTVE22X**
Weekly contact	**:**	**3 – 0 – 0 (L – T – P)**
Credit	**:**	**3**

Module	Topics
M1	**Introduction to RF Circuits:** Parallel RLC resonant networks, impedance matching, maximum power transfer theorem, RF front-end, image problem in receivers; direct-conversion receiver, noise, non-linearity, IIP3
M2	**Noise in CMOS Circuits:** Thermal Noise, Flicker Noise, Statistical Characteristics, Representation of Noise in Circuits, Noise in Current Mirror, Differential Amplifier, Noise-Power Trade-off, Noise Bandwidth
M3	**Low Noise Amplifier:** Important Parameters, Impedance Matching, Design Procedure, LNA Topologies, High-IP2 LNA, SGL0622Z LNA
M4	**Mixer:** Important Parameters, Design Procedure, Gilbert Cell, Down-conversion, Up-conversion
M5	**Power Amplifier:** Important Parameters, Classification, Design Procedure, High-Efficiency PA, Push-Pull Amplifier, Load-Pull Analysis, QPA9901 RF Power Amplifier
M6	**Voltage Controlled Oscillator:** Important Parameters, Design Procedure, Phase Noise, Tuning Range Limitations, Low-Noise VCO, LO Interface
M7	**Phase-Locked Loop:** Important Parameters, Design Procedure, Type-I and Type-II PLL, Phase Noise

Reference Books:

1. "CMOS: Circuit Design, Layout, and Simulation", R. Jacob Baker
2. "Design of Analog CMOS Integrated Circuits", Behzad Razavi
3. "The Design of CMOS Radio-Frequency Integrated Circuits", Thomas H. Lee
4. "RF Microelectronics", Behzad Razavi

Course Title	**:**	**5G and Wireless Technology**
Course Code	**:**	**MTVE229**
Weekly contact	**:**	**3 – 0 – 0 (L – T – P)**
Credit	**:**	**3**

Module	Topics
M1	**Introduction:** Major 5G enabling technologies : Introduction to 5G Communication Signals & System
M2	**Mobile Fading Channel:** Overview of Mobile Fading Channels, Smart Antennas and Mobile Generation of cellular systems- Free Space propagation, Multipath propagation, large scale and small scale fading, flat fading, selective fading, Doppler and motion initiated fading, fast and slow fading, Case Study of a Specific Wireless Channel. Overview of MIMO and Smart antennas and Beamformation, Millimeter Wave Communication for 5G Applications, Mobile Generation of cellular systems from 1G to 6G
M3	**5G Waveforms and Multiple Access:** Orthogonal Frequency Division Multiplexing (OFDM), Filter Bank Multi Carrier (FBMC), OFDMA and NOMA, 5G use Cases Slices- 5G eMBB (enhanced Mobile Broadband), 5G eMTC (Enhanced Machine Type Communications) and 5G URLLC (5G Ultra-Reliable and Low Latency Communication) Used Cases
M4	**5G Advanced Technology:** OPEN-RAN (O-RAN) SPLIT Architecture, Virtualization, 5G Core based SDN networking and CLOUD 5G OPEN RAN Introduction, Open RAN: Journey from Concept to Development, Evolution of the RAN,O-RAN Alliance Architecture, Open RAN Security Aspects, Network virtualization in 5G, 5G core and SDN , MEC and CLOUD
M5	**Advanced Technology:** O-RAN to B-RAN with AI automation and Blockchain security. Resource sharing and Multiple vendors use case of O-RAN: O-RAN updated to Blockchain enabled RAN (B-RAN) , B-RAN as a Service (BaaS), Case study of BRAN with AI automation and Blockchain security
M6	**Implementation:** Implementation of 5G Communication System. RAN TEST BEDs and DEMOs

Reference Books:

1. "Multiple Access Techniques for 5G Wireless Networks and Beyond", Mojtaba Vaezi, Zhiguo Ding, and H. Vincent Poor, Springer 2018, in process.
2. "Massive MIMO Networks: Spectral, Energy, and Hardware Efficiency", Emil Bj¨ornson, Jakob Hoydis, and Luca Sanguinetti, Foundations and Trends in Signal Processing, 2017.
3. "Cloud Mobile Networks: From RAN to EPC", by Mojtaba Vaezi, Ying Zhang, Springer 2017.
4. "Millimeter Wave Wireless Communications", Theodore S. Rappaport, Robert W. Heath, Robert C. Daniels, James N. Murdock, Prentice Hall, 2014 Digital Integrated Circuits: A Design Perspective", 4th Ed., Gray, Jan M Rabaey.

Course Title	**:**	**CAD for VLSI**
Course Code	**:**	**MTVE235**
Weekly contact	**:**	**3 – 0 – 0 (L – T – P)**
Credit	**:**	**3**

Module	Topics
M1	**Introduction:** Role of CAD in VLSI. Classification of VLSI: digital, analog, mixed signal, VLSI design flow, challenges
M2	**Verilog/VHDL:** Introduction and use in synthesis, modeling combinational and sequential logic, writing test benches
M3	**Logic synthesis:** Two-level and multilevel gate-level optimization tools, state assignment of finite state machines
M4	**Basic concepts of high-level synthesis:** Partitioning, scheduling, allocation and binding, Technology mapping
M5	**VLSI Technology and Design Styles:** Review of MOS/CMOS fabrication technology, various VLSI design styles: full-custom, standard-cell, gate-array and FPGA
M6	**Physical design automation algorithms:** Steps of VLSI Physical design processes, Partitioning: Kernighan-Lin (K-L) method, F-M Partitioning Method, ratio-cut method, Floorplanning: Slicing and Non-slicing floor planning, Simulated annealing method, Routing: Maze routing, Line-search method, Global routing and Channel routing, clock and power routing, etc
M7	**VLSI Testing:** Fundamentals of VLSI testing, automatic test pattern generation, design for testability, built-in self-test. Testing SoCs

Reference Books:

1. Douglas L. Perry, VHDL: Programming by Example 4th Edition, TMH.
2. R.H. Katz, "Contemporary logic design", Addison-Wesley Pub. Co., 995
3. M. S. Smith, "Application-specific integrated circuits", Addison-Wesley Pub. Co., 1997.
4. S. Rameshchandran, "Digital VLSI systems design", Springer, 2007.

Course Title : Embedded Systems Laboratory
Course Code : MTVE211
Weekly contact : 0 – 0 – 3 (L – T – P)
Credit : 3

List of Experiments:

Exp. No.	Topics
1	Design and development of Low Cost Embedded System using 8051 Microcontroller with Sensor/ Display/Actuator
2	Design and development of Low Cost Wireless Embedded System using 8051 Microcontroller with Sensor/ Display/Actuator with WiFi

3	Visualization of Signals out of Systems at Level 1 experiments using Digital Oscilloscope
4	Visualization of Signals out of Systems at Level 1 experiments using both Digital Oscilloscope and Spectrum Analyzer
5	Design and development of Embedded System using Arduino based 32-bit Microcontroller, leveraging ARM Cortex-M processors with Sensor/ Display/Actuator
6	Design and development of Embedded System using FPGA kit with Sensor/ Display/ Actuator
7	Write Python codes for Object Detection using 5G Camera
8	Simulation of a 5G gNB/ Core Network system by virtually connecting with Two UEs and communicating to one Internet Website.
9	To configure and show multimedia services at 5GTTH to the Home using 5G gNB, CPE and Home UE (Android TV Box)
10	PCB Design for ATmega328P-U PDIP-28 Microcontroller based Embedded Systems
11	Mini Project on Embedded Systems

Course Title : Mixed-Signal Laboratory
Course Code : MTVE212
Weekly contact : 0 – 0 – 3 (L – T – P)
Credit : 3

List of Experiments:

Exp. No.	Topics
1	Characterization of NMOS and PMOS Transistors
2	Design, Simulation, and Layout of Single-Stage Op-Amp
3	Design, Simulation, and Layout of Two-Stage Op-Amp
4	Design, Simulation, and Layout of Inverting and Non-Inverting Amplifiers
5	Design, Simulation, and Layout of Comparator
6	Design, Simulation, and Layout of Clocked Comparator
7	Design, Simulation, and Layout of Switched Capacitor Circuits

8	Design, Simulation, and Layout of DAC
9	Design, Simulation, and Layout of ADC
10	Design, simulation, and Layout of VCO
11	Mini Project on Mixed Signal IC Design

…….....…… END ……...……..…