

The VLSI Lab

(Funded by MeitY, Govt. of India)

Fostering Next Generation Capabilities Among Chip Designers For Making India Self-Reliant in **Electronics System Design**



UNLOCK The potential of innovation with cutting-edge VLSI design & advanced semiconductor solutions

Contact Us

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Institute C2S Server equipped with EDA Tools from Cadence / Synopsys / Mentor / Xilinx

FPGA Boards in Our Lab



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"Semiconductor engineering: Where electrons dance to the rhythm of innovation, paving the way for a brighter and more connected future."

Our Goals

- **Build Expertise:** Train students and researchers in SoC/system design to create industry-ready talent.
- Foster Collaboration: Strengthen partnerships with industry and academia for impactful R&D projects.
- **Promote Innovation:** Develop reusable IP cores and design ASICs/SoCs for societal and strategic applications.
- **Support Startups:** Incubate and mentor startups to drive entrepreneurship and innovation.
- Expand Research: Lead advancements in ASIC/IC design, engaging faculty, students, and startups.



Available EDA Tools Xilinx Vivado 2023 • UEF-MATSIM Cadence **OUANTUS** • SPECTRA • STARTUS • ASSURA • PVS222 • MODUS • CONFRML INCISIVE152 · XCELIUM • GENUS • IC 618 • PEGASUS • FOUNDRY • DDI221 • SSV221 • INTEGRAND• MVS211 SIGRITY • VMANAGER • LIBERATE • SPB • INNOVUS • JASPER Mentor • QUESTA • TANNER • OASYS • CALIBRE • TESSENT • NITRO **Synopsys** • FINESIM VU• ICVALIDATOR • SYN VT HSIMPLUS · NANOTIME • VCS HSPICE_VU PRIME_VT • SRARRC VU • ICC2 VU

Our Technical Team

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