Dated :- 31.07.19

BIDDING DOCUMENT

(TendorNo.IIITK/Tender/2019/98)

For Procurement of VLSI Design Software/Hardware for IIIT Kalyani

Subject :- Procurement of Software/Hardware for Computer Laboratory

IIIT Kalyani, an institute of national Importance, invites sealed Bids from Principal companies/ authorized distributors/bonafide suppliers who have adequate credential for Procurement of Software and Hardware for VLSI design for IIIT-Kalyani as per the details given below.

List of Software/Hardware

Sl.No.	Item	Description	No. of Licence/Units
1.	Software	FPGA Programming Software with Partial Reconfiguration : Specifications - Accelerating Implementation : Synthesis and Place and Route, Partial Reconfiguration Accelerating Verification: Vivado Simulator, Vivado Device Programmer, Vivado Logic Analyzer, Vivado Serial I/O Analyzer, Debug IP (ILA/VIO/IBERT) Accelerating High Level Design: Vivado High-Level Synthesis, Vivado IP Integrator, System Generator for DSP Make:- Xilinx Or Equivalent	Qty- 1set – (Latest Version, perpetual licenses) No of users- 25-30
2.	Hardware	FPGA Prototyping Boards 1:- FPGA Part Number :- XC7A35TICSG324-1L Logic Cells : - 32,280 Logic Slices :- 5,200 CMT : 5 Xilinx Artix-7 FPGA Internal clock speeds exceeding 450MHz On-chip analog-to-digital converter (XADC) Programmable over JTAG and Quad-SPI Flash System Features 256MB DDR3L with a 16-bit bus @ 667MHz 16MB Quad-SPI Flash Powered from USB or any 7V-15V source System Connectivity 10/100 Mbps Ethernet USB-UART Bridge Interaction and Sensory Devices 4 Switches	5 Units

		4 Buttons 1 Reset Button 4 LEDs 4 RGB LEDs Expansion Connectors 4 Pmod connectors Arduino/chipKIT Shield connector Make:- Xilinx or Equivalent	
		FPGA Prototyping Boards 2:- Xilinx ZynqSoC PYNQ Z2 XC7Z020-1CLG400C 650MHz dual-core Cortex-A9 processor DDR3 memory controller with 8 DMA channels and 4 High Performance AXI3 Slave ports High-bandwidth peripheral controllers: 1G Ethernet, USB 2.0, SDIO Low-bandwidth peripheral controller: SPI, UART, CAN, I2C Programmable from JTAG, Quad-SPI flash, and MicroSD card Programmable logic equivalent to Artix-7 FPGA 13,300 logic slices, each with four 6-input LUTs and 8 flip-flops 630 KB of fast block RAM 4 clock management tiles, each with a phase locked loop (PLL) and mixed-mode clock manager (MMCM) 220 DSP slices On-chip analog-to-digital converter (XADC) Memory 512MB DDR3 with 16-bit bus @ 1050Mbps 16MB Quad-SPI Flash with factory programmed 48-bit globally unique EUI-48/64™ compatible identifier MicroSD slot Power Powered from USB or 7V-15V external power source USB and Ethernet Gigabit Ethernet PHY Micro USB-JTAG Programming circuitry Micro USB-UART bridge USB 2.0 OTG PHY (supports host only) Audio and Video HDMI sink port (input) HDMI source port (output) I2S interface with 24bit DAC with 3.5mm TRRS jack Line-in with 3.5mm jack Switches, Push-buttons and LEDs 4 push-buttons 2 slide switches 4 LEDs	5 Units

		2 RGB LEDs Expansion Connectors Two standard Pmod ports 16 Total FPGA I/O (8 shared pins with Raspberry Pi connector) Arduino Shield connector 24 Total FPGA I/O 6 Single-ended 0-3.3V Analog inputs to XADC Raspberry Pi connector 28 Total FPGA I/O (8 shared pins with PmodA port) Make:- Xilinx Or Equivalent	

TERMS & CONDITIONS AND IMPORTANT INSTRUCTIONS FOR BIDDING

1) Bidders are to invited to submit sealed quotations on the official pad/letter head of the Company/authorized distributor/bonafide supplier as per the Technical Specifications for tendered items to office of Registrar , Indian Institute of Information Technology , Webel IT Park, Kalyani, Nadia, Pin Code - 741235, West Bengal between 11.00 am to 3.00 pm

2) The last date of receipt of tender is 21.08.2019. Quotations received later will not be entertained under any circumstances.

3) **EMD of Rs. 5000/- and tender fees of Rs. 500/- has to be submitted through separate Demand Draft in favour of Registrar, Indian Institute of Information Technology Kalyani.**

4) Date and Timing of opening the bid is the same day of receiving quotation at 3.30 pm and the place of opening of bid is office of IIIT Kalyani.

5) Bidders are to submit the quotations in sealed cover to the office in the Following address.

Registrar,
Indian Institute of Information Technology,
Webel IT Park, Kalyani
Nadia, Pin Code- 741235
West Bengal.

6) All bidders should submit in ONE-BID (TECHO-COMMERCIAL BID) in sealed envelope (Tender Number must be mentioned on envelope). The price quoted should be inclusive of all Taxes, duties, levies or any other charges to deliver items at the premises of the Institute. All taxes, freight, insurance charges, installation charges or any other specified overheads etc. should be clearly indicated . Inclusion of Tax/levy or any other charges at a later stage will not be accepted . At the end , the total price of a single item must be indicated as TOTAL PRICE: Rs.....only INCLUDING ALL.

7. Vendors must enclose attested copies of Trade licence, GST Registration, ISO Certificate , Last three years Income tax return, Tender Specific Authorization certificate from OEM, Vendor Should have Supplied Similar Item in at least four Academic Institutes in India Purchase order has to be enclosed, PAN Card or any other statutory testimonials etc. along with the bidding document, otherwise their tender will be cancelled.

8) The items must be supplied within a period of 07 days after the receipt of the purchase order

9) The materials are to be supplied at a place within IIITK s premises between 11.00 am and 4.00 pm. The tenderer will be responsible for any breakage, damage in item/product detected subsequently.

10) Bills in triplicate should be presented for payment within 15 days of supply/completion of work. **No Advance Payment can be Allowed.** All bills are to be accompanied by order copies and challan receipt. The order number is to be noted on both the challan and the Bill.

11) Documents to be submitted with the tender . Tender documents/Terms & Conditions in Original duly signed by the Proprietor/Partner/Director of the company as a token of acceptance of terms & conditions of Tender.

12)If there are any doubt please contact Dr. Debasish Bera (9163733456) between 2.00 pm - 4.00 pm. Bidders are advised to clear all doubts (if any) before submitting quotations. After submission the same, they shall not be entertained / not eligible to re-consider any issues under any circumstances.

We accept the above conditions.

Dated:

Signature of Bidders/Suppliers
with date & seal